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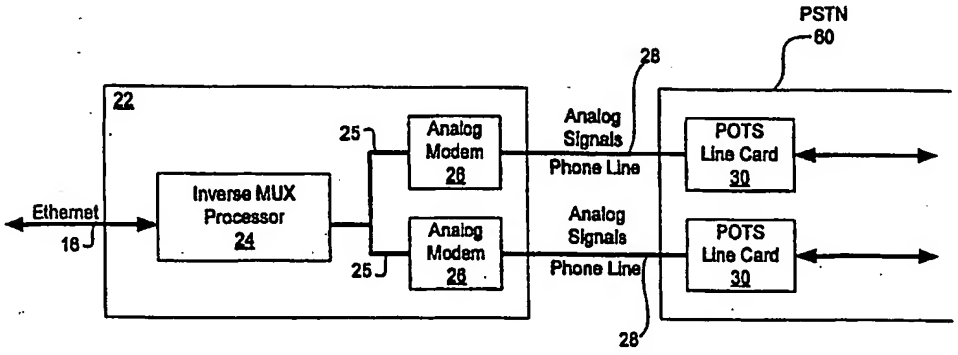

(57) Abstract

A bi–directional data communication system using inverse multiplexers for transmitting and receiving data at high–speeds using regular analog channels. The inverse multiplexer splits a high–speed digital signal into low–speed digital signals that are input to analog modems. The analog modems modulate the low–speed digital signals into low–speed analog signals for transmission over the analog channels to the public switched telephone network. At the remote end, the data carried by the analog channels is reverse inverse multiplexed into a high–speed digital signal by an inverse multiplexer operating in a reverse inverse multiplexing mode.

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SYSTEM FOR THE INVERSE MULTIPLEXING OF ANALOGUE CHANNELS

FIELD OF THE INVENTION

This invention relates to data communication systems, and more particularly to a system for transmitting and receiving data at high-speeds using regular analog channel connections to the public switched telephone network.

BACKGROUND OF THE INVENTION

As the demand for computer-based voice, video and data services increases, so does the demand for higher bandwidth. Networked technologies such as Integrated Services Digital Networks (ISDN), frame relay, Switched Multimegabit Digital Service (SMDS), Asynchronous Transfer Mode (ATM), satellite data communications systems, wireless communications systems and others have all been developed to meet this demand for bandwidth. To make these services universally available requires either a new communications network infrastructure, or significant modifications to the existing one. None of these systems offers users the ability to transmit and receive data at high speeds and low cost by using regular analog channel connections to the public switched telephone network.

A common low cost alternative for transmitting data is the conventional modem, which is designed to modulate and demodulate signals between a user's digital devices, and analog channels connected to the public switched telephone network. Conventional modems offer users the ability to send and receive data at speeds of up to 33.6 kbit/s, while a newer generation of modems offer users the ability to receive data at speeds of up to 56 kbit/s. Due to limitations inherent in ordinary analog channels, this is the maximum achievable data rate for a conventional analog modem.

An option that is open to a user who desires higher data rates includes making use of switched digital services offered by interexchange carriers and local exchange carriers. These services make it possible for a user to dial up point-to-point digital connections whose bandwidth ranges from 56 kbit/s to 3 Mbit/s and beyond. Examples of these switched digital services include Switched 56, Switched 64, Switched 384,

Switched 1536, and ISDN Multirate. However, the use of these switched digital services requires specialized digital access lines to the user's premises. The use of these digital access lines is commonly sold at a premium over the cost of a regular analog telephone line connected to a user's premises.

Another option open to a user who desires higher data rates is to make use of inverse multiplexing over digital data channels. Inverse multiplexing is a mechanism for aggregating multiple independent data channels across a network to create a single higher rate data channel. The equipment that performs inverse multiplexing is called an inverse multiplexer. A user desiring a higher data rate would use an inverse multiplexer to aggregate multiple calls that have been set up using the switched digital services described above. For example, if six different independent 56 kbit/s data channels are established between points A and B in a network, an inverse multiplexer can be used to combine these channels to create a single 336 kbit/s (ie. 6 X 56 = 336) data stream. Likewise, 64, 384 and 1536 kbit/s channels can be inverse multiplexed together. Inverse multiplexers are sold by equipment vendors such as Ascend Communications, Inc, Nortel™, and U.S. Robotics™.

The most common example of inverse multiplexing that is made available to users is the ISDN Basic Rate Interface (BRI). An ISDN BRI specifies an ISDN line that has two 64 kbit/s data and voice (B) channels, and one 16 kbit/s signalling (D) channel. The two B channels are inverse multiplexed together to provide the user with a single high-speed 128 kbit/s channel. However, as was the case with switched digital services, specialized digital access lines to the user's premises are required to take advantage of the capabilities of inverse multiplexing. In addition to the extra costs levied by telephone companies to use digital access lines, a further disadvantage is that these digital access lines are not available in every area where local phone service is provided.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide a data communication system that combines the high-speed capabilities of inverse multiplexing with the low cost benefits of conventional analog modems. This object is achieved by a bi-directional data communication device comprising an inverse multiplexer having a high-speed side and a low-speed side, a plurality of analog modems each having a first terminal connected in common to the low-speed side of the inverse multiplexer and each having a second terminal whereby a high-speed digital signal input to the high-speed side of the inverse multiplexer is output on the second terminal of the modems as a plurality of low-speed analog signals and vice versa.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a prior art inverse multiplexer used to inverse multiplex two ISDN channels;

Figure 2 is a block diagram of the inverse multiplexer of the present invention used to inverse multiplex two analog channels;

Figure 3 is a detailed block diagram of the inverse multiplexer of the present invention;

Figure 4 is a block diagram of the inverse multiplexer of the present invention used to inverse multiplex two analog channels to a remote end having an analog connection to the public switched telephone network;

Figure 5A is a block diagram of the inverse multiplexer of the present invention used to inverse multiplex two analog channels to an Internet Service Provider at the remote end having an ISDN PRI connection to the public switched telephone network;

Figure 5B is a block diagram of the inverse multiplexer of the present invention used to inverse multiplex two analog channels to an Internet Service Provider at the remote end having a T1 connection to the public switched telephone network;

Figure 6 is a block diagram showing the present invention being operated by a stand-alone personal computer;

Figure 7 is a block diagram showing the present invention being operated in a router arrangement; and,

Figure 8 is a block diagram showing the present invention being operated in a router and bridge arrangement.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows a prior art inverse multiplexer 10 being used to inverse multiplex a high-speed digital signal 16. The prior art inverse multiplexer 10 shown in Figure 1 is used in a data communication system that is digital end-to-end. Though Figure 1 shows an end-to-end digital communication system based on ISDN, similar prior art systems are also used in association with other end-to-end digital communication systems such as Switched 56, Switched 64, Switched 384, Switched 1536. In this case, the inverse multiplexer microprocessor 12 receives a high-speed digital signal 16 and splits it into two low-speed digital signals 25 for transmission across two ISDN channels 18. An ISDN interface 14 is provided to interface between the inverse multiplexer 10 and the ISDN line cards 20 which are part of the public switched telephone network (PSTN) 60. The digital signals 25 transmitted on the two low-speed ISDN channels 18 are then transmitted over the PSTN 60 to the remote end (not shown) where they are reverse inverse multiplexed into one high-speed digital signal. The ISDN channels 18 are typically sold to users at a premium over the cost of a Plain Old Telephone System (POTS) line 28, 29 in Figure 2 connected to the Public Switched Telephone Network. While only two low-speed digital signals 25 are shown in Figure 1, prior art inverse multiplexers have the capability to split a high-speed digital signal 16 into any number of low-speed digital signals. The high-speed digital signal 16 shown in Figures 1, 2, 3, 4, 5A and 5B may be carried across a number of transmission lines, including an ethernet line.

Figure 2 shows an inverse multiplexer 22 of the present invention. Rather than being used in a data

communication system that is digital end-to-end, the inverse multiplexer 22 of the present invention is designed to inverse multiplex a high-speed digital signal 16 into a plurality of analog signals for transmission across analog channels 28, 29 to the PSTN 60. The analog channels 28, 29 would most commonly be comprised of regular POTS telephone lines of the type used to transmit voice traffic from the user's premises to the PSTN 60. As a result, there is no premium associated with the use of these analog channels 28, 29 as compared to the cost of a digital access line such as ISDN. The user need only pay for the use of the n POTS lines from its premises to the PSTN 60, where n is the number of analog channels 28, 29 required to meet the bandwidth requirements of the high-speed digital signal 16 to be inverse multiplexed in accordance with the present invention.

In operation, a high-speed digital signal 16 is input to an inverse multiplexer microprocessor 24, which is responsible for setting up analog channels 28, 29 as required, providing end-to-end ordering, delay compensation, and synchronization with the remote end (not shown). This functionality is provided by software executing standardized communications protocols on the inverse multiplexer microprocessor 24. The inverse multiplexer microprocessor 24 splits the high-speed digital signal 16 into two low-speed digital signals 25 that are input to two analog modems 26. The analog modems 26 modulate the low-speed digital signals into two low-speed analog signals for transmission over the analog channels 28, 29 to POTS line cards 30 which are part of the PSTN 60. The operation of the present invention is not dependent on the manner in which the analog signals are transmitted across the PSTN 60 to the remote end. Data carried by channels 28, 29 are transmitted across the PSTN 60 in accordance with whatever transmission and switching means is employed by the PSTN 60, either digital, analog, or some combination thereof. At the remote end, the data carried by channels 28, 29 is reverse inverse multiplexed by an inverse

multiplexer identical to inverse multiplexer 22 but operating in a reverse inverse multiplexing mode.

The present invention is bi-directional, in that it is also utilized to receive data from the remote end on a plurality of low-speed analog channels 28, 29 to be reverse inverse multiplexed into one high-speed digital signal 16. Although only two analog channels 28, 29 are shown in Figure 2, the present invention can be used to inverse multiplex a high-speed digital signal into any number of analog signals carried by analog channels 28, 29. The number of analog channels 28, 29 required is dependent on the data rate of the high-speed digital signal 16 to be inverse multiplexed, and the speed of the analog modems 26. For each additional analog channel to be accommodated, there would be required one additional analog modem 26.

There is no upper or lower limit on the speed of the analog modems used in accordance with the present invention. In the preferred embodiment, a plurality of 56 kbit/s analog modems 26 are connected to the inverse multiprocessor 24. This permits the rate of the high-speed digital signal 16 to operate at a speed of up to n X 56 kbit/s, where n is the number of 56 kbit/s analog modems used. Persons skilled in the art will appreciate that present day 56 kbit/s analog modems 26 are asymmetric, which means that where the remote end has a direct digital connection to the PSTN 60, 56 kbit/s analog modems can receive data at a rate of up to 56 kbit/s, though can only transmit data at a rate of up to 33.6 kbit/s, and vice versa. The 56 kbit/s analog modems that operate in accordance with the present invention are compatible with both the K56Plus™ standard developed by Rockwell International™, and the X2™ standard developed by U.S. Robotics™.

Analog modems 26 that can transmit and receive data at lower speeds, such as 33.6 kbit/s, may also be used in accordance with the present invention. For example, if three 56 kbit/s analog modems 26 were employed by the inverse multiplexer 22, the maximum data rate of the aggregated channel would be 3 X 56 kbit/s, or 168 kbit/s. The present invention

will function with analog modems 26 operating at any data rate, not only with modems operating at data rates of 56 kbit/s, or 33.6 kbit/s.

Figure 3 is a detailed block diagram of the inverse multiplexer 22 of the preferred embodiment of the present invention. Within the inverse multiplexer 22 is a microprocessor 24 with integral ethernet hardware interface (not shown), a block of non-volatile read-only memory (ROM) 34, a block of read/writable memory (RAM) 36 and at least two analog modem chips 26. Though only two analog modem chips 26 are shown, the inverse multiplexer 22 of the present invention can accommodate up to n analog modem chips 26, where n is the number of analog channels 28, 29 required to meet the bandwidth requirements of the high-speed digital signal 16. Connecting these devices together is a (address:data:control) bus 38 which moves data and control information to and from the analog modem chips 26. Not shown, but which may be present, are minor support logic, such as a reset circuit, clock oscillator and block selection logic.

Stored within the ROM memory 34 is software for performing standardized inverse multiplexing protocol and other functions. The RAM 36 is used for data buffering and other data store.

In the preferred embodiment, inverse multiplexing is performed using the PPP Multilink Protocol (MP). This protocol is capable of splitting, recombining, and sequencing the transmission and reception of data on multiple channels. The purpose of the PPP Multilink Protocol is to establish the channels to be used for the connection between the user's premises and the remote end, determine how the receiving inverse multiplexer (not shown) will reorder the incoming data from the individual channels, and how it will compensate for the relative delays between channels. The PPP Multilink Protocol is described in Internet Engineering Task Force (IETF) Request for Comments (RFC) 1990. A standardized protocol is used to assure interoperability with the equipment on the remote end of the transmission. By using standard inverse

multiplexing protocols, a user may send and receive data from equipment located at the remote end that may be manufactured by a vendor different from the vendor who manufactured the user's inverse multiplexing equipment.

In addition to software running standardized inverse multiplexing protocol, there may be specialized software resident in the ROM 34 designed to provide an interface between the inverse multiplexer microprocessor 24 and the analog modem chips 26, to turn the system on and off, setup the system, initiate dialing, etc.

Figure 4 illustrates the inverse multiplexer of the present invention used to inverse multiplex a high-speed digital signal 16 into a plurality of analog signals for transmission across analog channels 28, 29 to a remote end 68 having analog connection 100, 101 to the PSTN 60. The detail included in Figure 2 relating to the POTS line card 30 is excluded from Figure 4 for the purposes of clarity. In the embodiment of the invention illustrated in Figure 4, the remote end 68 includes a configuration of devices 26, 27 that is the mirror image of the configuration of devices 24, 26 located at the user's premises.

To operate the inverse multiplexer 22 shown in Figure 4, the user would place a telephone call over analog channel 28 across the PSTN 60, over analog channel 100, to the receiving inverse multiplexer microprocessor 27. To ensure interoperability, the receiving inverse multiplexer microprocessor 27 must be set-up to transmit and receive data using the same protocol as that employed by the calling inverse multiplexer microprocessor 24 located at the user's premises. When channel 28, 60, 100 is established, and the receiving inverse multiplexer 27 confirms that it is capable of supporting multilink connections, the initiating multiplexer microprocessor 24 requests addition of another link to the connection. When the receiving multiplexer processor 27 agrees to the establishment of another link 29, 60, 101, the initiating multiplexer processor 24 will establish a connection on the second link. After the appropriate network layer

protocol has been negotiated between the multiplexer processors 24, 27 and the second link has been established, the data traffic may be exchanged over the multilink connection.

In accordance with the inverse multiplexing protocol employed by the inverse multiplexer microprocessor 24, the high-speed digital signal 16 is split into two low-speed digital signals and framed for transmission across analog channels 28, 29, across the PSTN 60, through analog channels 100, 101, to the remote end 68. The signals on the analog channels 28, 29 are transmitted across the PSTN 60 in accordance with whatever transmission and switching means is employed by the PSTN 60, either digital, analog, or some combination thereof. If the PSTN 60 is a digital network, equipment located at the end of the PSTN 60 nearest to the calling inverse multiplexer microprocessor 24 must perform an analog-to-digital conversion of the signals carried by the analog channels 28, 29 for transmission and switching across the PSTN 60. As well, equipment located at the end of the PSTN 60 nearest to the receiving inverse multiplexer microprocessor 27 must perform a digital-to-analog conversion to reconstitute the signals carried by analog channels 28, 29 into their remote end counterparts 100, 101.

Signals transmitted over analog channels 100, 101 are received by the analog modems 26 located at the remote end, and demodulated for transmission to the receiving inverse multiplexer microprocessor 27. In accordance with the PPP Multilink Protocol, the receiving inverse multiplexer microprocessor 27 re-aggregates or reverse inverse multiplexers the data into a high-speed digital signal compensating for any relative delays between channels. The receiving inverse multiplexer microprocessor 27 will insert framing data into the high-speed digital signal 16 in accordance with whatever transmission line is used at the remote end. For example, ethernet framing data will be inserted into the high-speed digital signal 16 if an ethernet line is used to transmit the high-speed digital signal 16. Once the communication is terminated, the calling inverse multiplexer microprocessor 24

performs the necessary signalling functions to remove channels 28, 29, 100, 101. The system illustrated in Figure 4 is bi-directional, such that the inverse multiplexer microprocessors 24, 27 can operate as both a calling inverse multiplexer microprocessor, and a receiving inverse multiplexer microprocessor.

In the embodiment illustrated in Figure 4, the maximum data rate for each analog modem 26 is 33.6 kbit/s. Data rates above 33.6 kbit/s (e.g. 56 kbit/s) can only be achieved where the remote end has a direct digital connection to the PSTN 60 (as illustrated in Figures 5A and 5B). Where the remote end does not have a direct digital connection to the PSTN (as illustrated in Figure 4), quantization noise introduced by analog-to-digital converters that form part of the PSTN 60 impair transmission and reception such that the maximum data rate achievable by an analog modem 26 is only 33.6 kbit/s. This means that where two analog modems 26 are employed in the configuration illustrated in Figure 4, the maximum achievable data rate would be 2 X 33.6 kbit/s, or 67.2 kbit/s. Due to their asymmetric nature, where the remote end has a direct digital connection to the PSTN 60 (as illustrated in Figures 5A and 5B), present day 56 kbit/s analog modems can receive data at a rate of up to 56 kbit/s, though can only transmit data at a rate of up to 33.6 kbit/s, and vice versa.

Figure 5A illustrates the inverse multiplexer of the present invention used to inverse multiplex two analog channels 28, 29 to an Internet Service Provider (ISP) at the remote end 44 having an ISDN PRI 62 connection to the PSTN 60. In this case, the remote end 44 may be an ISDN access switch. The distinction between the embodiment of the present invention illustrated in Figure 5A as compared to the embodiment illustrated in Figure 4 is that the remote end 44 has a direct digital connection 62 to the PSTN 60. While an ISDN Primary Rate Interface (PRI) digital connection 62 is illustrated in Figure 5A, the present invention can be used in association with any digital connection to the PSTN 60, such as a T1, as illustrated in Figure 5B. In addition, it is to be understood

that the processor 27 illustrated in Figures 5A and 5B is generally more powerful than the processor 27 illustrated in Figure 4. This is because the processor 27 illustrated in Figures 5A and 5B must be designed to handle up to 24 channels, whereas the processor 27 illustrated in Figure 4 may be required to handle only two channels, though it may be capable of handling up to n channels, where n is the number of analog channels 100, 101 required to meet the bandwidth requirements of the high-speed digital signal 16.

In the embodiment of the invention illustrated in Figure 5A, the remote end 44 includes a configuration of components 67, 64, 66, 27 designed to deal with the direct digital connection 62 to the PSTN 60. In this case, analog signals carried by low-speed analog channels 28, 29 across the PSTN 60 are received by an ISDN PRI interface 64 which splits the ISDN PRI 62 line into 24 component 64 kbit/s digital channels. In the receive direction, the ISDN PRI interface 64 separates the ISDN PRI bit stream into 23 "B" channels, and one "D" channel for subsequent processing by other components inside the switch located at the remote end 44. In the transmit direction, the ISDN PRI interface 64 combines signals to form 23 "B" channels, and one "D" channel, and transmits the combined signal onto the ISDN PRI line 62.

The individual 64 kbit/s digital channels will then be routed to either a pool of ISDN interfaces 66, or a pool of digital modems 67. Since the signals originating from the user's premises are not ISDN signals, the ISDN PRI interface 64 will route the 64 kbit/s channels containing the data originating with the user in quantized digital format to the pool of digital modems 67 connected to a receiving inverse multiplexer microprocessor 27. The digital modems 67 demodulate the signals transmitted from the ISDN PRI interface 64 into digital signals for use by the receiving inverse multiplexer microprocessor 27. When digital signals are received from the receiving inverse multiplexer microprocessor 27 (when, for example, user data is flowing from the remote end 44 to inverse multiplexer 22), the digital modems 67 will

modulate the digital signals into waveforms in quantized digital format for use by the ISDN PRI interface 64.

Using the same standardized protocol employed by the calling inverse multiplexer microprocessor 24, the receiving inverse multiplexer microprocessor 27 reverse inverse multiplexes the data received from the digital modems 67 into a high-speed digital signal. The system illustrated in Figure 5A is bi-directional, such that the inverse multiplexer microprocessors 24, 27 can operate as both a calling inverse multiplexer microprocessor, and a receiving inverse multiplexer microprocessor, even though the system typically operates in the receiving mode.

Figure 5B illustrates the inverse multiplexer of the present invention used to inverse multiplex two analog channels 28, 29 to an ISP at the remote end 45 having a T1 connection to the PSTN 60. The distinction between the embodiment of the present invention illustrated in Figure 5B as compared to the embodiment illustrated in Figure 5A is that the remote end 45 has a T1 63 connection to the PSTN 60, rather than an ISDN PRI 62 connection. In the embodiment of the invention illustrated in Figure 5B, the remote end 45 includes a configuration of components 65, 67, 27 designed to deal with the T1 connection 63 to the PSTN 60. In this case, analog signals carried by low-speed analog channels 28, 29 across the PSTN 60 are received by T1 interface 65 which splits the T1 line into 24 component 64 kbit/s digital channels which are routed to a pool of digital modems 67. Using the same standardized protocol employed by the calling inverse multiplexer microprocessor 24, the receiving inverse multiplexer microprocessor 27 reverse inverse multiplexes the data into a high-speed digital signal. As in Figures 4 and 5A, the system illustrated in Figure 5A is bi-directional, such that the inverse multiplexer microprocessors 24, 27 can operate as both a calling inverse multiplexer microprocessor, and a receiving inverse multiplexer microprocessor, even though the system typically operates in the receiving mode.

Figure 6 illustrates the present invention being operated by a stand-alone personal computer 82, 84. With respect to personal computer 82, the inverse multiplexer 22 is located internally, whereas with respect to personal computer 84, the inverse multiplexer 22 is located externally. The configuration of the communications equipment illustrated in Figure 6 is applicable to a single user who is using the present invention to transmit and receive data to/from the Internet, or a private network through an access switch 80. The access switch 80 may be configured in a number of ways, including the configurations 44, 45 illustrated in Figures 5A and 5B. By combining the data rates of the analog channels 28, 29 connected to the user's premises, the user may transmit and receive data from the Internet and/or private network at high-speeds, without the need for a specialized digital access line. Instead, a user need only purchase access to the required number of analog lines necessary to carry the user's data traffic. The cost of these additional analog lines is typically less than the cost of a specialized digital access line such as ISDN BRI.

Figures 7 and 8 show different configurations for the devices supported by the present invention. In Figure 7, the present invention is shown being operated in a router arrangement. In this configuration, the inverse multiplexer router 41 directs data packets to and from a variety of devices, such as personal computers 82 and a laser printer 86 via an ethernet cable 46. The access switch 80 may be configured in a number of ways, including the configurations 44, 45 illustrated in Figures 5A and 5B. In this configuration, an inverse multiplexer router 41 is capable of transmitting and receiving data originating from, or destined to any of the devices 82, 86 connected to the ethernet cable 46.

Figure 8 is a block diagram showing the present invention being operated in a router and bridge arrangement. In the configuration, the inverse multiplexer bridge 50 is connected on one side via an ethernet connection 46 to a

plurality of devices, such as personal computers 82 and a laser printer 86. On the other side, the inverse multiplexer bridge 50 is connected via a plurality of analog channels 54 to its peer 52. The inverse multiplexer bridges 50, 52 are used to pass data traffic between segments of the network at high-speeds using only analog channels 54. In the configuration shown in Figure 8, the inverse multiplexer bridges 52 are themselves connected to each other and to a variety of devices, such as personal computers 82, a laser printer 86, and an inverse multiplexer router 41 via an ethernet cable 46. In this configuration, the inverse multiplexer router 41 is capable of transmitting and receiving data originating from, or destined to any of the devices 82, 86 connected to the ethernet cable 46, or the inverse multiplexer bridges 50, 52, or the access switch 80.

We Claim:

1. A bi-directional data communication device comprising an inverse multiplexer having a high-speed side and a low-speed side, a plurality of analog modems each having a first terminal connected in common to the low-speed side of the inverse multiplexer and each having a second terminal whereby a high-speed digital signal input to the high-speed side of the inverse multiplexer is output on the second terminal of the modems as a plurality of low-speed analog signals and vice versa.

2. The bi-directional data communication device of claim 1 wherein the analog modems are connected to respective analog lines connected to the public switched telephone network.

3. The bi-directional data communication device of claim 2 wherein the inverse multiplexer includes means for establishing a connection with the internet or other computer network.

4. The bi-directional data communication device of claim 3 wherein the analog modems are each capable of receiving data at a rate of 56 kbit/s.

5. The bi-directional data communication device of claim 1, 2, 3, or 4 wherein the inverse multiplexer comprises a microprocessor, a block of non-volatile read-only memory, a block of read/writable memory (RAM) all connected to each other by a bus.

6. The bi-directional data communication device of claim 5 wherein the analog modems are connected to the inverse multiplexer by the bus.

7. A bi-directional data communication system comprising a first inverse multiplexer and a second inverse multiplexer,

said first inverse multiplexer operating as a calling inverse multiplexer when said second inverse multiplexer is operating as a receiving inverse multiplexer and said first inverse multiplexer operating as a receiving inverse multiplexer when said second inverse multiplexer is operating as a calling inverse multiplexer, said first and second inverse multiplexers each comprising: a high-speed side and a low-speed side, said low-speed side being connected to the public switched telephone network on a plurality of parallel analog lines, circuitry for inverse multiplexing a high-speed digital signal input to said high-speed side into a plurality of low-speed digital signals and vice versa, a plurality of analog modems connected in common to said circuitry for modulating said low-speed digital signals into a plurality of low-speed analog signals and vice versa, whereby a high-speed digital signal input to the high-speed side of the calling inverse multiplexer is output on the low-speed side of the calling inverse multiplexer as a plurality of low-speed analog signals which are transmitted on said analog lines through the public switched telephone network to the low-speed side of the receiving inverse multiplexer, and output on the high-speed side of the receiving inverse multiplexer as a high-speed digital signal.

8. The bi-directional data communication device of claim 7 wherein at least one of the first inverse multiplexer and the second inverse multiplexer are connected to the internet or other computer network.

9. A bi-directional data communication system comprising a first inverse multiplexer and a second inverse multiplexer, said first inverse multiplexer operating as an calling inverse multiplexer when said second inverse multiplexer is operating as a receiving inverse multiplexer and said first inverse multiplexer operating as a receiving inverse multiplexer when said second inverse multiplexer is operating as a calling inverse multiplexer, said first and second inverse multiplexers each comprising a high-speed side and a low-speed side, said

low-speed side of said first inverse multiplexer being connected to the public switched telephone network on a plurality of parallel analog lines, and said low-speed side of said second inverse multiplexer being connected to the public switched telephone network on at least one digital line, said first inverse multiplexer further comprising: circuitry for inverse multiplexing a high-speed digital signal input to said high-speed side into a plurality of low-speed digital signals and vice versa, a plurality of analog modems connected in common to said circuitry for modulating said low-speed digital signals into a plurality of low-speed analog signals and vice versa, means for converting and multiplexing said low-speed analog signals into corresponding digital signals for transmission through the public switched telephone network; said second inverse multiplexer further comprising: interface means for receiving said corresponding digital signals from the public switched telephone network on said digital line, circuitry for reverse inverse multiplexing said corresponding digital signals into a high-speed digital signals and vice versa, whereby a high-speed digital signal input to the high-speed side of the calling inverse multiplexer is output on the low-speed side of the calling inverse multiplexer as a plurality of low-speed analog signals which are transmitted on said analog lines through the public switched telephone network to the low-speed side of the receiving inverse multiplexer on said digital line, and output on the high-speed side of the receiving inverse multiplexer as a high-speed digital signal.

10. The bi-directional data communication device of claim 9 wherein at least one of the first inverse multiplexer and the second inverse multiplexer are connected to the internet or other computer network.

11. The bi-directional data communication system of claim 9 or 10 whereby the interface means is an ISDN Primary Rate Interface.

12. The bi-directional data communication system of claim 9, 10 or 11 wherein the interface means is a T1 interface.

13. A method of transmitting a high-speed digitally encoded signal originating at a customer's premises along analog lines to the public switched telephone network, comprising the steps of:

transmitting a high-speed digital signal to an inverse multiplexer;

inverse multiplexing said high-speed digital signal into a plurality of low-speed digital signals;

transmitting said plurality of low-speed digital signals in parallel to respective analog modems;

modulating said low-speed digital signals in said analog modems into a plurality of low-speed analog signals;

transmitting said low-speed analog signals along said analog lines and through the public switched telephone network.

14. A method of receiving a high-speed digitally encoded signal originating at a customer's premises and transmitted along low-speed analog lines through the public switched telephone network, comprising the steps of:

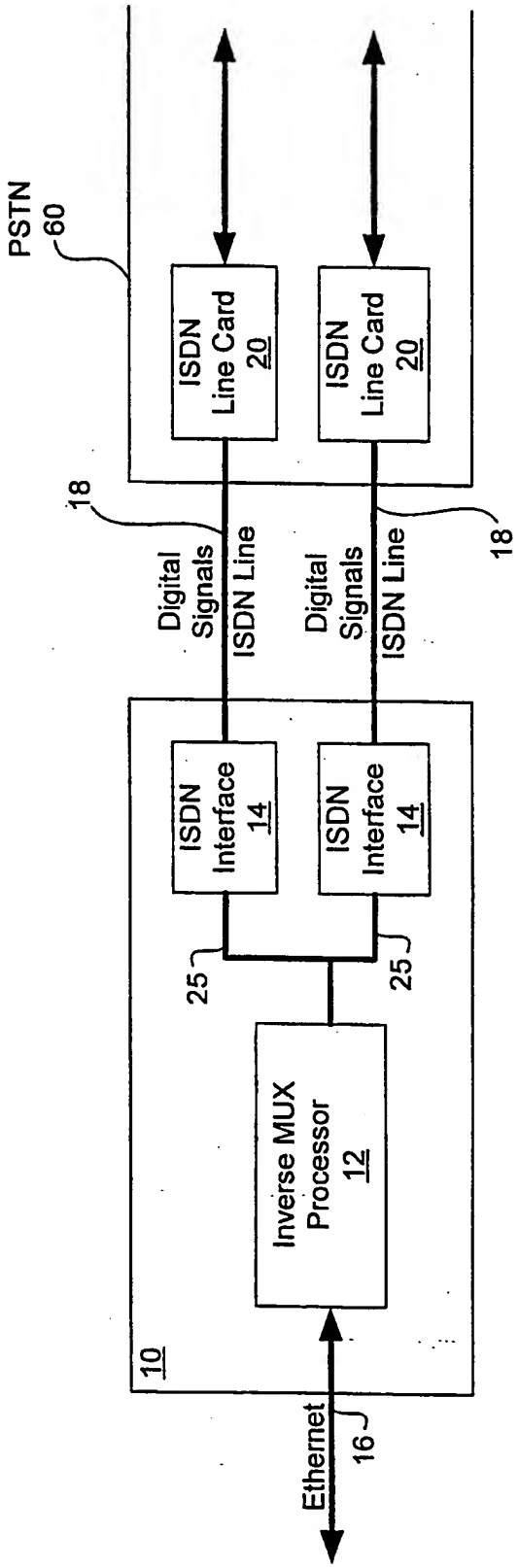
receiving a plurality of low-speed analog signals from the public switched telephone network;

transmitting in parallel said plurality of low-speed analog signals to respective analog modems;

demodulating said low-speed analog signals in said analog modems into a plurality of low-speed digitally encoded signals;

reverse inverse multiplexing said low-speed digital signals into a high-speed digitally encoded signal.

Figure 1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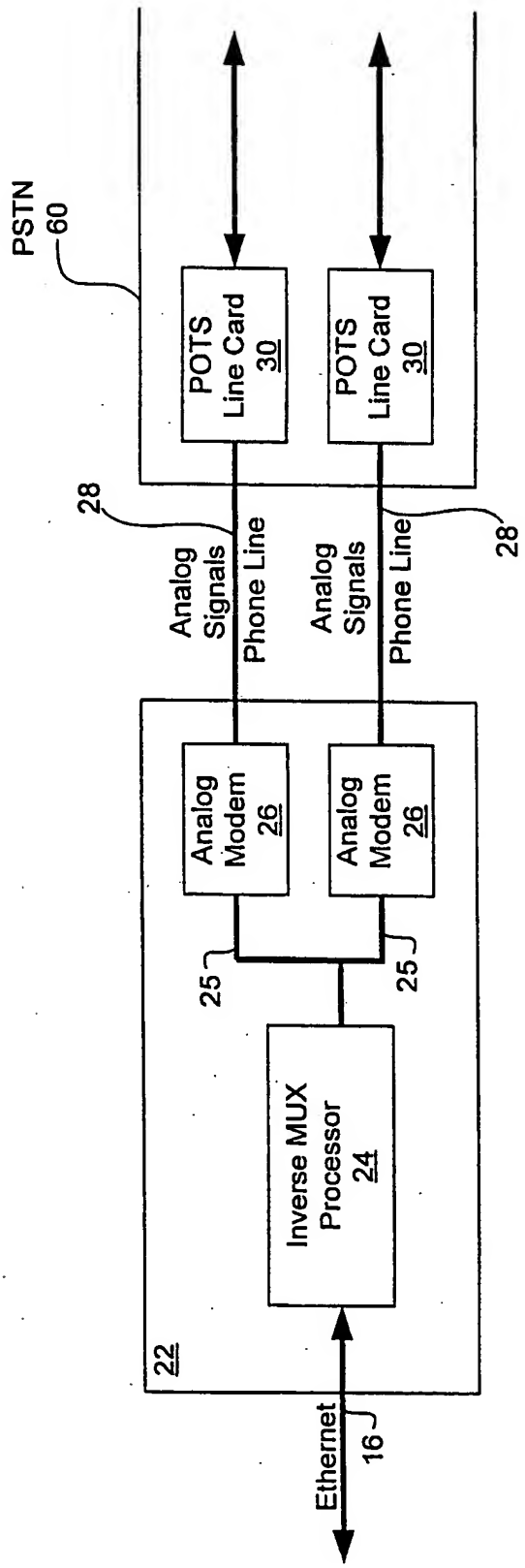
ISDN Line Card 20
ISDN Line Card 20
18
18
Digital Signals
ISDN Line
Digital Signals
ISDN Line
ISDN Interface 14
ISDN Interface 14
25
25
Inverse MUX Processor 12
10
Ethernet
16

Figure 2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POTS Line Card 30
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28
Analog Signals
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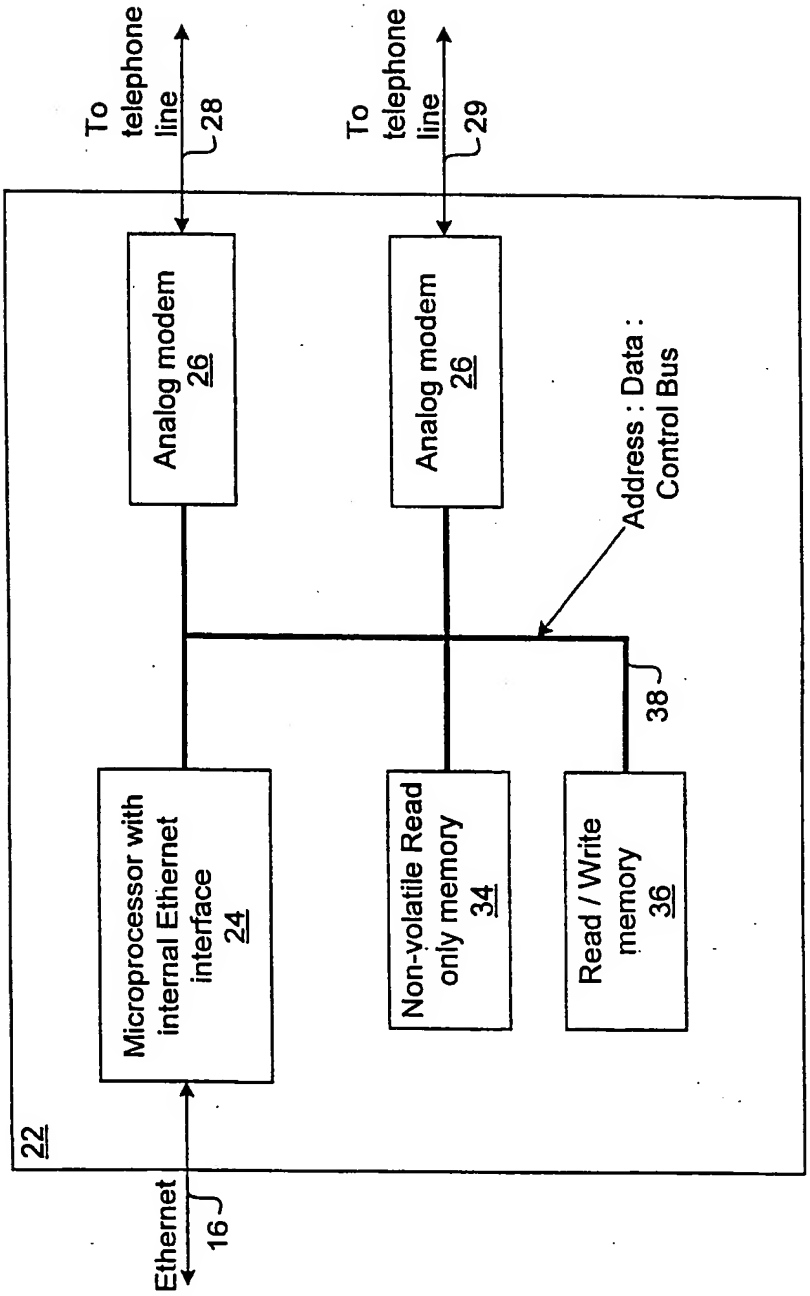
Analog Signals
Phone Line
Analog Modem 26
Analog Modem 26
25
25
Inverse MUX Processor 24
22
Ethernet
16

Fig. 3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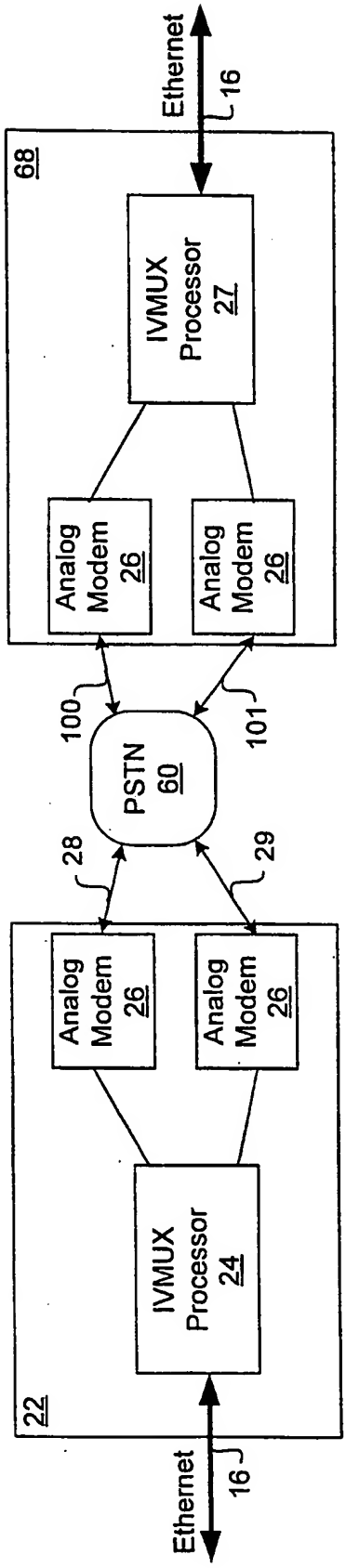
To telephone line 29
Analog modem 26
Analog modem 26
Address : Data : Control Bus
38
Microprocessor with internal Ethernet interface 24
Non-volatile Read only memory 34
Read / Write memory 36
22
Ethernet 16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IVMUX Processor 27
Analog Modem 26
Analog Modem 26
100
101
PSTN 60
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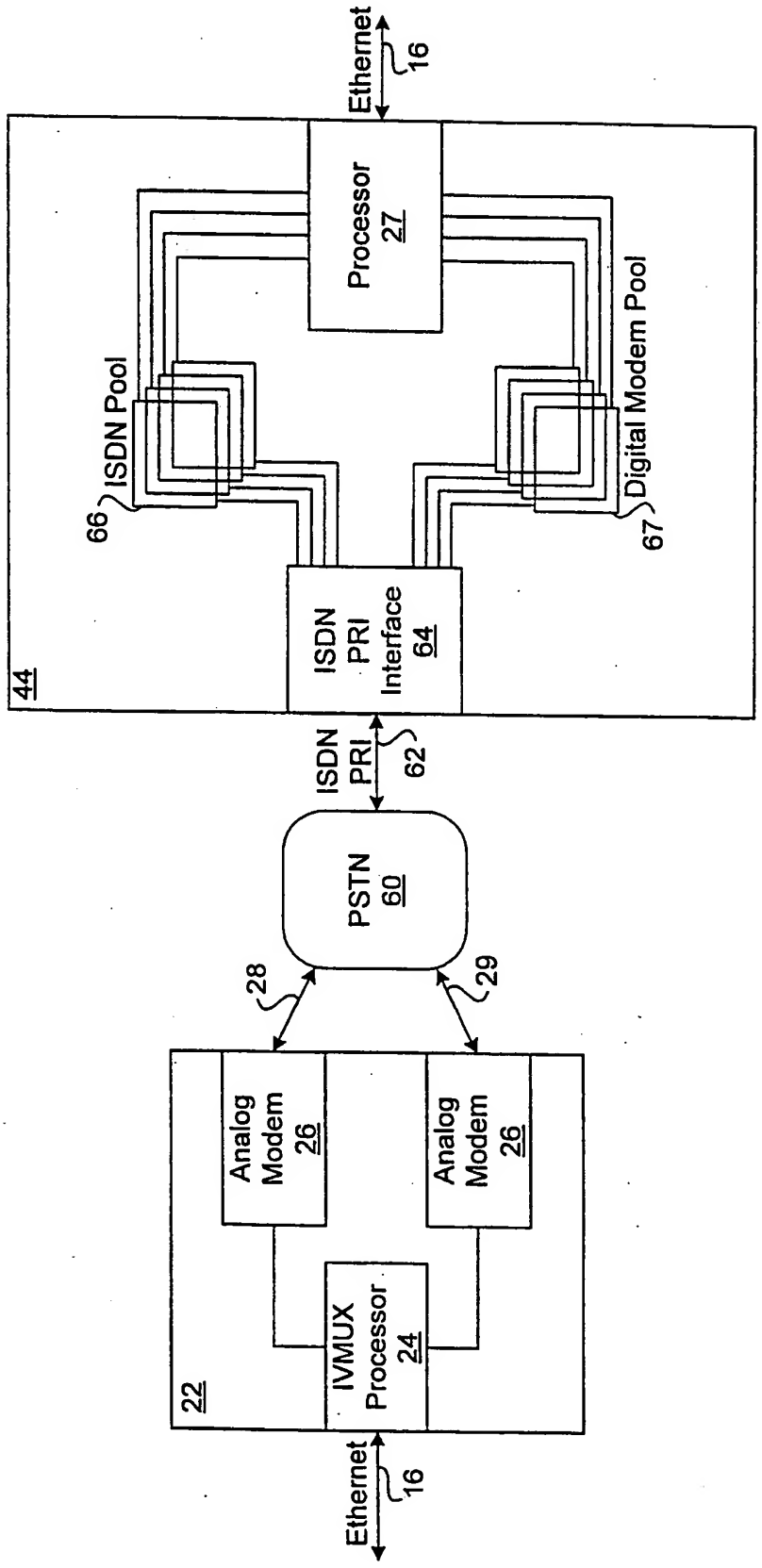
29
Analog Modem 26
Analog Modem 26
IVMUX Processor 24
22
Ethernet
16

Fig. 4

Fig. 5a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Processor
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ISDN Pool
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Digital Modem Pool
67
ISDN
PRI
Interface
64
44
ISDN
PRI
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PSTN
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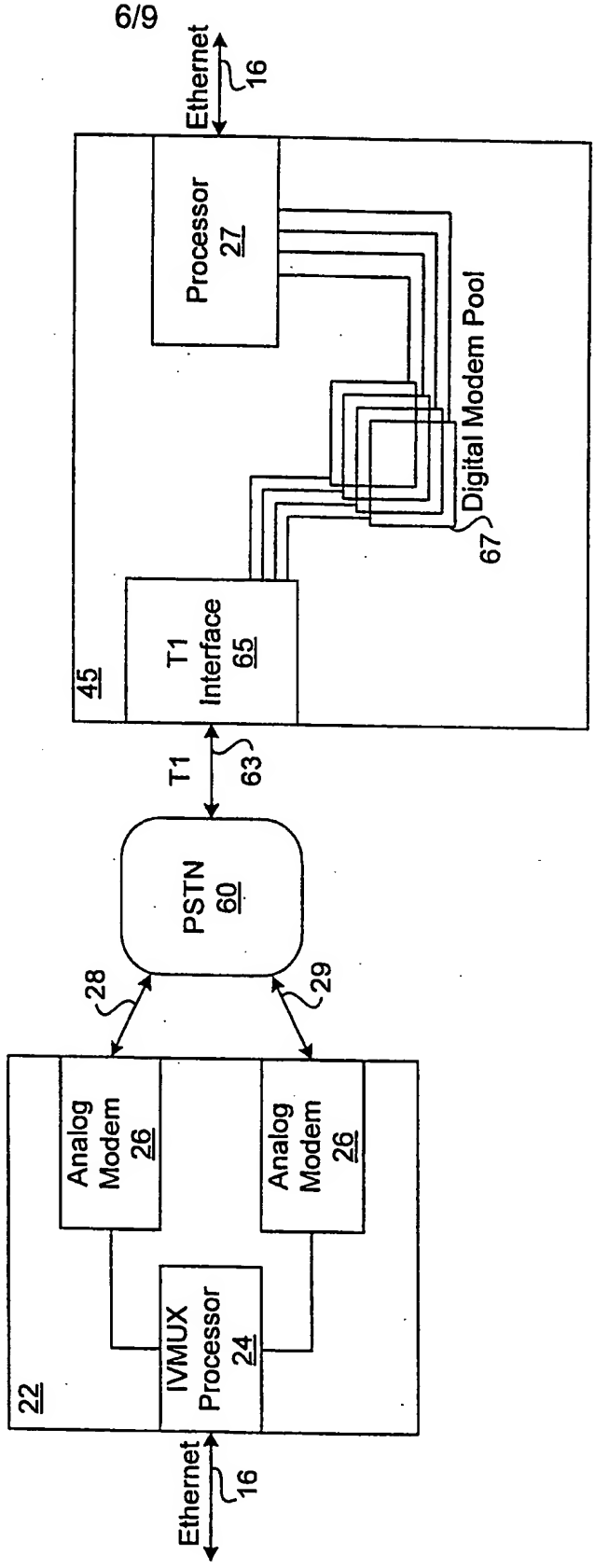
Analog
Modem
26
Analog
Modem
26
IVMUX
Processor
24
22
Ethernet
16


Ethernet
16
Processor
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Digital Modem Pool
67
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T1
Interface
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T1
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PSTN
60
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Analog
Modem
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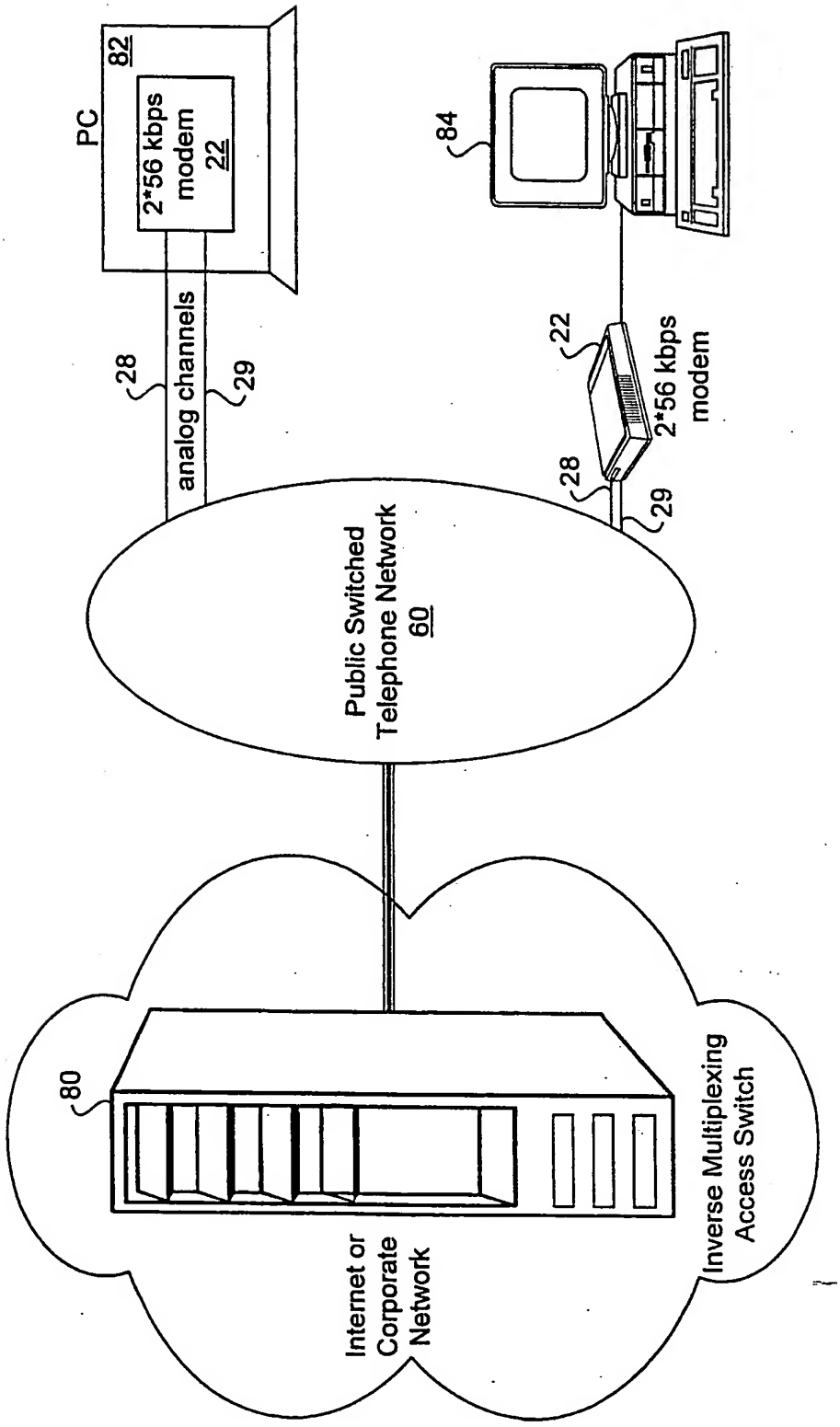
Analog
Modem
26
IVMUX
Processor
24
22
Ethernet
16

Fig. 5b

Fig. 6


PC
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2*56 kbps
modem
22
analog channels
28
29
84
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2*56 kbps
modem
28
29
Public Switched
Telephone Network
60
80
Internet or
Corporate
Network
Inverse Multiplexing
Access Switch

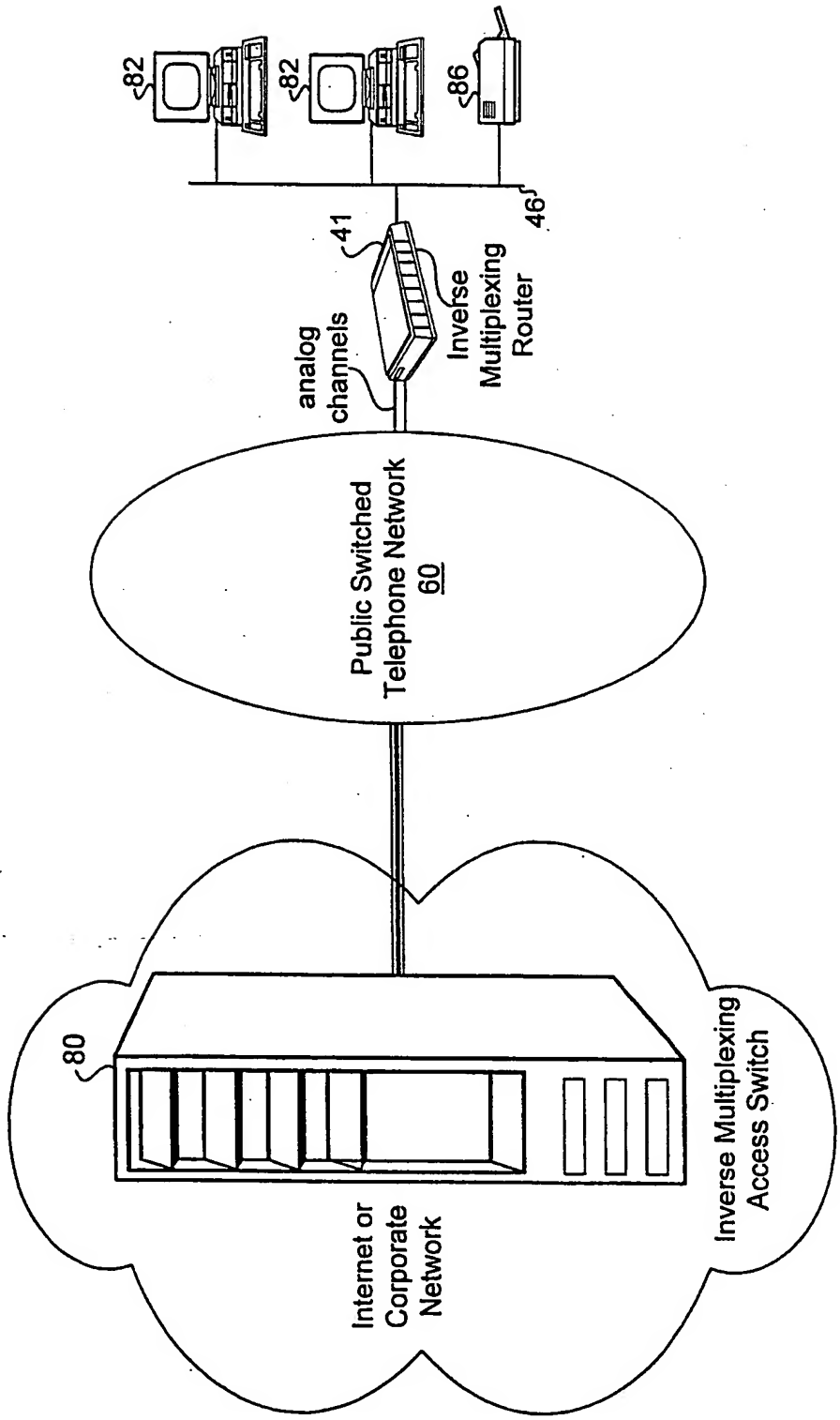
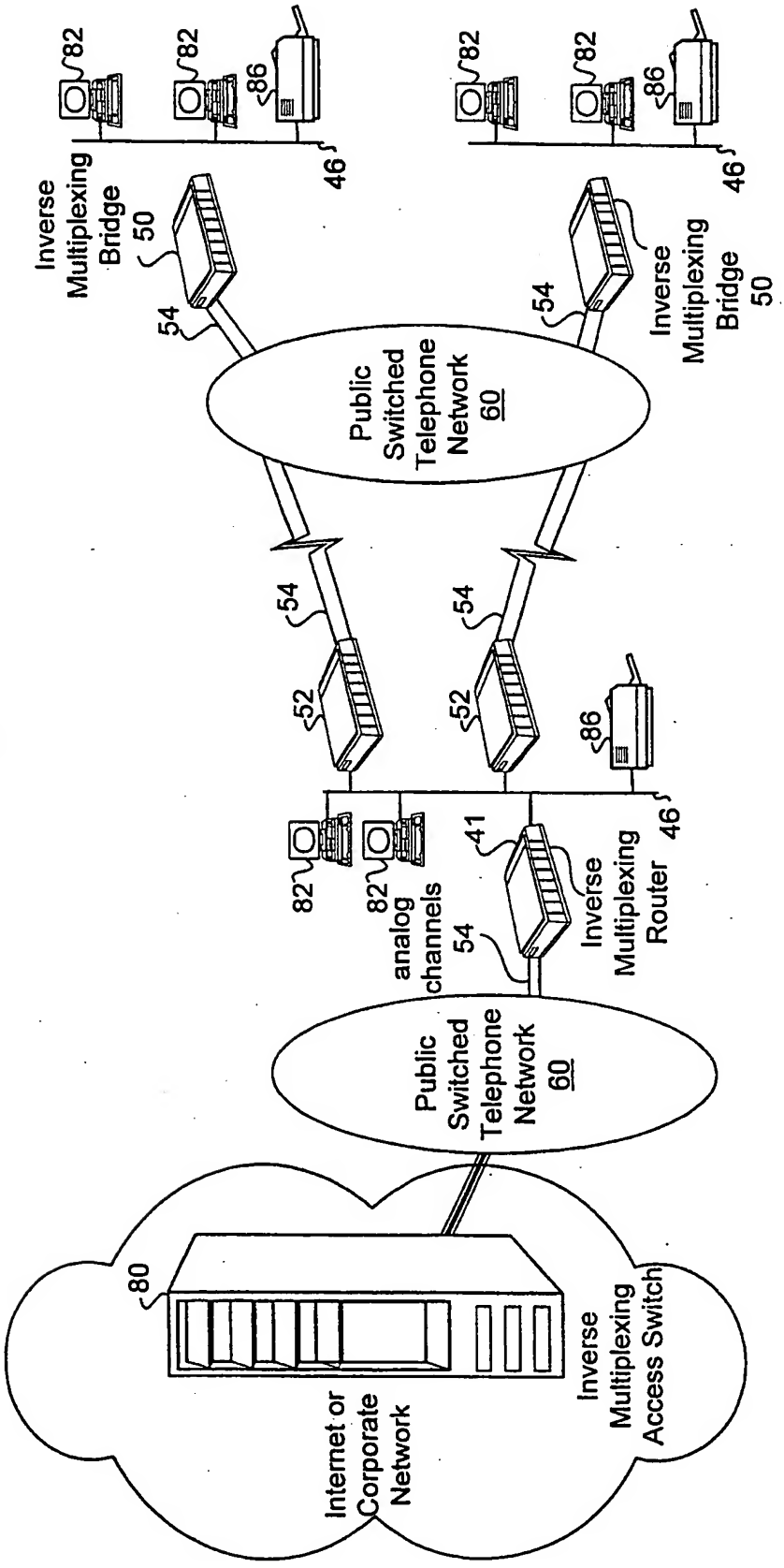

82
82
86
46
41
Inverse Multiplexing Router
analog channels
Public Switched Telephone Network 60
80
Internet or Corporate Network
Inverse Multiplexing Access Switch

Fig. 7

Fig. 8


Inverse Multiplexing Bridge 50
82
82
86
46
54
Public Switched Telephone Network 60
52
analog channels
Inverse Multiplexing Router
41
Internet or Corporate Network
80
Inverse Multiplexing Access Switch

INTERNATIONAL SEARCH REPORT

In ıtional Application No
PCT/CA 98/00103

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L25/14 H04L12/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 864 567 A (GIORGIO) 5 September 1989 see column 1, line 17 - line 27 ---	1-14
X	WO 93 07727 A (DIGITAL ACCESS) 15 April 1993 see page 1, line 9 - line 14 see page 7, line 25 - line 32 see page 11, line 3 - line 7 see page 5, line 28 - line 34 see page 6, line 4 - line 12 see page 14, line 9 - line 15 see page 16, line 25 - page 17, line 2 see page 17, line 8 - line 12 --- -/--	1-14

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 August 1998	01/09/1998

Name and mailing address of the ISA	Authorized officer
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1

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INTERNATIONAL SEARCH REPORT

national Application No
PCT/CA 98/00103

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 93 02514 A (DIGITAL ACCESS) 4 February 1993 see page 1, line 17 - line 21 see page 8, line 19 - page 9, line 4 see page 14, line 25 - page 15, line 6	1-14
X,P	WO 97 32415 A (ENCANTO NETWORK) 4 September 1997 see page 2, line 2 - line 7 see page 2, line 14 - line 24 see page 3, line 9 - line 12 see page 4, line 15 - line 16	1-14

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 98/00103

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		US 5491695 A	13-02-1996
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